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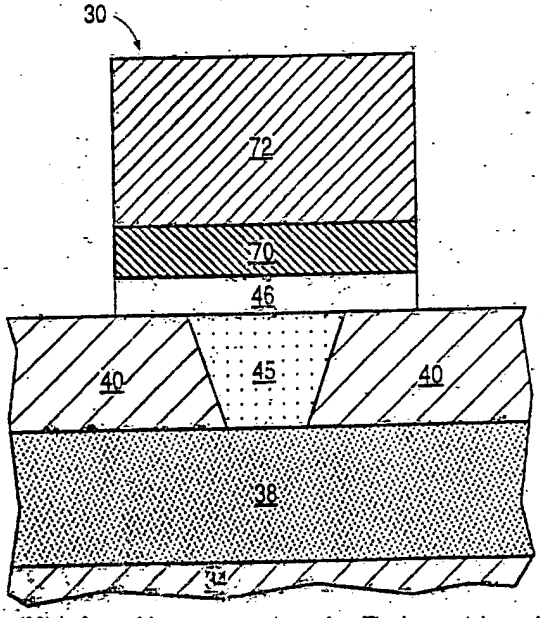

(57) Abstract

An amorphous silicon antifuse (30) is formed between two electrodes. The bottom electrode (45) is a plug, of tungsten in one embodiment, formed in a via in a dielectric layer (40). The top surface of the plug is coplanar with the top surface of the dielectric layer. Thus the amorphous silicon layer above the plug is planar, as is the top electrode layer above the amorphous silicon. Deposition of the amorphous silicon (46) and of the top electrode is facilitated thereby. The electrical characteristics of the antifuse are tightly controlled. The antifuse has a simple structure, a small size, small capacitance in the unprogrammed condition, and small leakage current. The antifuse can be made with relatively few process steps. The process sequence provides a planar top surface for the amorphous silicon deposition and the top electrode (70, 72) formation.

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AMORPHOUS SILICON ANTIFUSES AND METHODS FOR FABRICATION THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to programmable integrated circuit structures and methods for fabrication thereof, and more particularly to amorphous silicon antifuses and circuits and routing structures incorporating antifuses, and methods for fabrication thereof.

Description of Related Art

Programmable semiconductor devices include programmable read only memories ("PROMs"), programmable logic devices ("PLDs"), and programmable gate arrays. Programmable elements suitable for one or more of these device types include fuses and antifuses.

A fuse is a structure which electrically couples a first terminal to a second terminal, but which, when programmed by passage of sufficient current between its terminals, electronically decouples the first terminal from the second terminal. A fuse typically is of a conductive material which has a geometry that causes portions of the conductive fuse material to physically separate from each other when heated to the extent that an open circuit results.

An antifuse is a structure which when unprogrammed does not electrically couple its first and second terminals, but which, when programmed by applying sufficient voltage between the first and second terminals, permanently electrically connects the first and second terminals. One type of antifuse comprises an amorphous silicon which forms conductive polysilicon when heated.

In BROM devices, for example, the advantages of the antifuse technology over fuse technology include scalability and reduced programming current requirement. Various antifuses are disclosed in United States Patent No. 3,675,090, issued July 4, 1972 to Neale, and United States Patent No. 3,792,319, issued February 12, 1974 to Tsang.

The use of amorphous silicon in the fabrication of semiconductor threshold and switch devices is well known. As more fully discussed in the aforementioned Neale patent, various semiconductor switch devices comprise a "pore" filled with amorphous silicon, which contacts a lower electrode forming surface and an upper electrode forming surface.

Neale recognized the two important objectives were to obtain switch devices with a very low leakage current in the preprogrammed condition and a fairly consistent programming voltage value. An aspect of the Neale invention was to fabricate the semiconductor switch device so as to present a very small cross-sectional area of semiconductor material for current flow to minimize leakage current paths therethrough.

Antifuses have been used successfully in programmable interconnect substrates, memories, and some types of PLDs. See, for example, U.S. Patent No. 4,458,297, issued July 3, 1984 to Stopper et al.

An example of antifuse technology for a bipolar BROM is illustrated in Figures 1 and 2, which are taken from Brian Cook and Steve Keller, "Amorphous Silicon Antifuse Technology for Bipolar PROMs," 1986 Bipolar Circuits and Technology Meeting, 1986, pp. 99-100.

In the via antifuse of Figure 1, first metal comprising aluminum conductor 14 and barrier metal 10 and 11 is provided on an oxide layer 13 overlaying substrate 12. A thick oxide layer 18 is provided over conductor 14 as insulation from second metal. A via etched into oxide layer 18 is lined with a thin film of amorphous silicon

15, which fully overlays and contacts the barrier metal 11 under the via. Second metal comprising barrier metal 16 and aluminum conductor 17 is provided over the via, in contact with the amorphous silicon 15.

The contact antifuse of Figure 2 is formed over a transistor comprising collector 20, base 21, and emitter 22. Emitter contact is made to a platinum silicide region 23 through a contact hole in oxide 24, which is lined with amorphous silicon film 25. Barrier metal 26 and aluminum conductor 27 overlay the amorphous silicon 25, and are protected by oxide 28.

In the examples of Figures 1 and 2, the deposition of the amorphous silicon was a critical step in the process, as the thickness of the film 15 (Figure 1) and film 25 (Figure 2) was thought to control the programming voltage. The pre-programmed leakage current was reduced to about 6 microamperes at 2 volts by a high temperature anneal at 450 degrees C. Other factors thought to influence leakage current in the undoped amorphous silicon antifuse were feature size (leakage current proportional) and film thickness (leakage current inversely proportional).

Unfortunately, antifuse technology developed for use in memories is generally too leaky for use in PLDs, as noted by Cook et al. In a PROM, one bit is selected per output at a time; therefore, if the programmable elements are leaky, only one leaky bit loads the sense amplifier. Usually the sense amplifier can tolerate this loading without drastically affecting its functionality or performance. Contrast one type of PLD known as a programmable array logic, which is implemented using PROM technology. The programmable elements are used to configure logic (routing is dedicated and global). In programmable array logic, multiple bits can be accessed and may overload the sense line if the programmable elements are leaky. Overloading the sense line may drastically degrade the performance and in the extreme case, may result in functional failure.

Certain techniques have been employed in PLDs using antifuse technology to overcome the problems created by antifuse leakage. One technique uses active semiconductor devices such as diodes or transistors to block the leakage current, an approach which can also be used in memories having leaky antifuses. While this approach is satisfactory in memories and in the logic configuration circuits of PLDs, the technique is not satisfactory for use in the routing circuits of such integrated circuits as the field programmable gate array ("FPGA").

The FPGA, which is distinguished from conventional gate arrays by being user programmable, otherwise resembles a conventional gate array in having an interior matrix of logic blocks and a surrounding ring of I/O interface blocks. Logic functions, I/O functions, and routing of interconnect networks are all user configurable, which affords high density and enormous flexibility suitable for most logic designs. User logic, for example, conventionally is implemented by interconnecting two-input NAND gates into more complex functions. Extensive user configurability of the FPGA is achieved by incorporating a large number of programmable elements into the logic and the I/O blocks and the interconnect network. Naturally, the leakage requirement of the programmable elements is stringent, due to the large number of possible connections generally involved and the numerous failure modes that leakage can cause. For instance, leaky programmable elements in the routing areas contribute to high supply current problems, cross talk problems, and performance degradation.

It is desirable to provide an easily manufacturable amorphous silicon antifuse which has a simple structure, a small size, small capacitance in the unprogrammed condition, small leakage current, and highly reproducible physical and electrical characteristics, and which is suitable for use in FPGAs.

SUMMARY OF THE INVENTION

Some embodiments of the amorphous silicon antifuses of the present invention have a simple structure, a small size, small capacitance in the unprogrammed condition, small leakage current, and highly reproducible and controllable physical and electrical characteristics. Their manufacture requires very few process steps, and the process sequence provides a planar top surface for almost all the steps. In particular, the amorphous silicon is planar in some embodiments so that a high quality, uniform thickness deposition thereof is facilitated. The electrode overlaying the amorphous silicon is also planar in some embodiments, and the electrode fabrication is thereby facilitated.

These and other advantages are achieved in some embodiments of the antifuse structure according to the present invention. The structure generally includes a dielectric layer having an opening therethrough; a conductive plug filling the opening, a top surface of the plug being substantially coplanar with a top surface of the dielectric layer; an amorphous silicon layer overlaying and contacting the plug; and a conductor overlaying and contacting the amorphous silicon layer.

Further, a method is provided for fabricating an antifuse structure. The method generally includes the steps of fabricating an insulating layer; fabricating an opening through the insulating layer at a selected location; fabricating a plug of conductive material in the opening so that a top surface of the plug is substantially coplanar with a top surface of the insulating layer; fabricating a layer of amorphous silicon overlaying and contacting the plug; and fabricating a conductor overlaying and contacting the amorphous silicon layer.

The invention further provides a programmable interconnect structure, a field programmable gate array, and a method for fabricating a field programmable gate array.

These and other embodiments of the invention are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, where like referenced numerals indicate like parts,

Figures 1 and 2 are cross-section illustrations of prior art amorphous silicon antifuse structures;

Figures 3-5 are cross-section illustrations of intermediary structures of the processes of manufacturing an amorphous silicon antifuse according to the present invention;

Figure 6 is a cross-section illustration of an amorphous silicon antifuse of the present invention; and

Figure 7 is a cross-section illustration of a portion of a programmable CMOS integrated circuit having an amorphous silicon antifuse in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figures 3-6 illustrate the basic steps of fabricating an antifuse structure that can be used, among other things, with programmable semiconductor devices. The final structure, an amorphous silicon antifuse 30, is illustrated in Figure 6. As shown in Figure 3, a first dielectric layer 34, typically of silicon dioxide, is formed on a silicon substrate (not shown), and patterned to expose portions of the substrate. Alternatively, the dielectric layer 34 may be formed over other film layers (not shown) or features such as conductors (not shown) rather than directly on the substrate. A first conductive layer 38 is formed on dielectric layer 34 and patterned to form appropriate interconnects. In one embodiment, the first conductive layer 38 is a layer of aluminum. In another embodiment, the first conductive layer 38 is TiW. In still another embodiment, the first conductive layer 38 comprises various conductive layers (not shown), including

a thin layer of titanium covered by a thicker layer of aluminum. Other conductive layers are suitable as well.

A second dielectric layer 40 is formed on the first conductive layer 38. The second dielectric layer 40 is patterned to form vias, such as via 44, exposing the first conductive layer 38. Some of these vias, in particular via 44, will serve as sites for antifuses. Other vias, not shown, may allow for direct connection between first conductive layer 38 and a to-be-formed second conductive layer.

As shown in Figure 4, a plug 45 of conductive material is formed in via 44 so as to fill the via. Plug 45 provides the bottom electrode of the antifuse. The top surface of the plug 45 is substantially coplanar with the top surface of the second dielectric layer 40. Consequently, a to-be-formed amorphous silicon layer 46 (Figure 6) will be planar. Formation of high quality, uniform layer 46 is thereby facilitated.

In one embodiment, the plug 45 is made of tungsten. Tungsten plugs have been used to provide interlevel contacts between different conductive layers. Any suitable tungsten plug deposition technique may be used. For example, in one technique, the plug 45 is formed by selective chemical vapor deposition ("CVD") of tungsten in the via 44. At the bottom of via 44, the material of first conductive layer 38 reacts with gaseous reactants so as to form tungsten in via 44. No tungsten is deposited, however, on top of the second dielectric layer 40 during the selective CVD. Selective CVD of tungsten is described generally in R.V. Joshi et al., "Low-Resistance Submicron CVD W Interlevel Via Plugs on Al-Cu-Si," VMIC Conference, June 12-13, 1989, pp. 113-121, available from the Institute of Electrical and Electronic Engineers ("IEEE") of Piscataway, New Jersey and hereby incorporated herein by reference thereto. See also T. Ohba, "Selective and Blanket Tungsten Interconnection and its Suitability for 0.2-Micron ULSI," VMIC Conference, June 12-13, 1990,

pp. 226-232, available from IEEE and hereby incorporated herein by reference thereto; T. Moriya et al., "A Planar Metallization Process--Its Application to Tri-Level Aluminum Interconnection," 83 IEDM 550, hereby incorporated herein by reference thereto.

In another technique, the plug 45 is formed by a blanket CVD of tungsten followed by etch-back. As shown in Figure 5, the blanket CVD of tungsten provides tungsten layer 45 with a planar top surface. The layer 45 is etched until tungsten is etched off the top of the second dielectric layer 40. In a variation, a thin adhesion layer of TiW (not shown) is sputtered on the surface of the via 44 before the blanket CVD of the tungsten layer 45 of Figure 5. In another variation, a sacrificial layer of silicon nitride (not shown) is deposited on top of the second dielectric layer 40 before the via 44 is formed. The silicon nitride protects the surface of the second dielectric layer 40 and reduces the loading effects during the etch of the tungsten layer 45 of Figure 5. After the etch, the remaining silicon nitride is removed. Tungsten plug formation by blanket CVD and etch-back is generally described in J.M.F.G. van Laarhoven et al., "A Novel Blanket Tungsten Etchback Scheme," VMIC Conference, June 12-13, 1989, pp. 129-135, available from IEEE and hereby incorporated herein by reference thereto.

In another variation, the plug 45 is formed by selective CVD of tungsten into the lower portion of the via 44 and then by the blanket CVD of tungsten and an etch-back so as to fill up the via 44. See generally T. Ohba et al., supra.

As shown in Figure 6, layer 46 of amorphous silicon is deposited and patterned over the via 44. Layer 46 is planar, and deposition of high quality amorphous silicon having uniform thickness and consistent, easily reproducible physical and electrical characteristics is thereby facilitated. As is explained in application Serial No. 07/447,969, filed December 8, 1989, whose

disclosure is hereby incorporated herein by reference thereto, the thickness of amorphous silicon layer 46 in contact with the plug 45 is an important factor in controlling the programming voltage and leakage current of the antifuse. In this embodiment, the thickness of amorphous silicon layer 46 is about 1,600 angstroms. Of course, other thicknesses are suitable depending on the programming voltage desired.

As described in the above-mentioned application Serial No. 07/447,969, another factor controlling leakage current is the manner of deposition of the amorphous silicon layer 46. In one embodiment, the amorphous silicon layer 46 is deposited using plasma enhanced chemical vapor deposition ("PECVD"). A suitable reactor is the Concept One reactor available from the Novellus Systems, Inc., San Jose, California. Suitable reactants and process parameters are described generally in the above-mentioned application Serial No. 07/447,969.

As shown in Figure 6, the second electrode of the antifuse 30 is formed by sputter depositing an about 2,000 angstrom layer 70 of titanium tungsten (TiW) and an about 8000 angstrom layer 72 of aluminum-copper (AlCu). TiW layer 70 and AlCu layer 72 are patterned to form the second electrode. The mask used for patterning the second electrode layers 70 and 72 is smaller than the mask used to pattern the amorphous silicon 46 so that, in the worst misalignment case, the entire second electrode is above amorphous silicon 46. Portions of the amorphous silicon 46 that are exposed by the second electrode mask are etched away when layers 70 and 72 are etched during the second electrode formation.

Layers 70 and 72 are planar above the amorphous silicon layer 46. The planarity facilitates deposition of layers 70 and 72. TiW layer 70 is a barrier layer that serves to prevent the aluminum of AlCu layer 72 from spiking into the amorphous silicon 46. Aluminum spikes would increase the leakage current or might even cause a

short across the antifuse 30.

As is seen from the above disclosure, the antifuse 30 can be fabricated using fairly few process steps. Further, the process sequence provides a planar top surface for the amorphous silicon deposition and the top electrode formation. Since the amorphous silicon layer 46 and the second electrode layers 70 and 72 are planar, a high quality uniform deposition of layers 46, 70 and 72 is facilitated. Further, if plug 45 is made of tungsten, no barrier layer between the amorphous silicon 46 and the first conductive layer 38 is needed even if aluminum is used in the first conductive layer 38.

The use of plug 45 as the bottom electrode allows to reduce the overall area of the antifuse 30 because a high quality plug with a good contact to first conductive layer 38 can be formed even when via 44 is narrow relative to the thickness of the second dielectric layer 40. Because of the small area of antifuse 30, leakage current and the capacitance of the unprogrammed antifuse are reduced. Further, in field programmable gate arrays with thousands or millions of antifuses, even a small size reduction of each antifuse may provide a significant overall size reduction of the FPGA. The second dielectric layer 40 can be made quite thick so as to reduce the capacitance between the first conductive routing channels formed from the first conductive layer 38 and the second conductive routing channels formed from TiW layer 70 and AlCu layer 72.

A cross-sectional view of a portion of a CMOS programmable gate array structure having an antifuse in accordance with the embodiment of Figure 6 is illustrated in Figure 7. Suitable CMOS processes are well known and commercially available, and the particular CMOS structure shown is exemplary. The antifuse 30 of Figure 6 can be used in integrated circuit structures of any type formed by any process, whether memory, logic, digital or analog, and including NMOS, PMOS, Bipolar, BICMOS, Gallium

Arsenide, and others.

Substrate 100 is provided with a P-doped substrate region 104. An NMOS device 162 that forms part of logic or I/O circuits of the gate array comprises source and drain regions 112 and 114 and gate 116. Patterned oxide layers 118, 119 and 120 (shown in cross hatch) also are present. As is well known in the art, oxide layer 118 is a field oxide, boro-phosphosilicate glass layer 119 is a contact oxide, and oxide layer 120 comprises various oxide layers (not shown) formed in the fabrication of gate 116. The oxide layers 118, 119 and 120 are suitably patterned and etched to form contact holes down to the various source and drain regions including regions 112 and 114.

Using standard techniques, a film of aluminum measuring about 6,000 angstroms is sputtered over the patterned oxide layers and into the contact holes to regions 112 and 114. Other metals may be used as well. Aluminum film 38 corresponds to the first conductive layer 38 of Figures 3-6. First metal lines are formed by patterning and etching aluminum film 38 using a BCl_3, Cl_2, $CHCl_3$ standard aluminum dry etch.

The intermetal dielectric is a thick oxide layer 40 of about 9,000 angstroms thickness, deposited using any suitable standard technique such as, for example, plasma enhanced chemical vapor deposition. Layer 40 corresponds to the second dielectric layer 40 of Figures 3-6. In one of many suitable techniques, the layer 40 comprises two oxide layers (not shown). The first oxide layer is deposited to the selected thickness and planarized. The planarization step involves spinning a resist layer over the deposited oxide and reflowing the resist with a postbake, after which the surface is planarized in an RIE etch-back adjusted for equal resist and oxide etch rates. A second oxide layer then is deposited to ensure dielectric integrity and the 9,000 angstrom thickness over the irregular topography.

Antifuse vias 44a and 44b are now formed through the

oxide 40 down to the aluminum film 38. An antifuse via mask having the same dimension as the metal opening mask is used to pattern the oxide, and vias are etched to the Al film 38 using standard RIE techniques.

Conductive plugs 45a, 45b are formed in the respective vias 44a, 44b. Plugs 45a, 45b provide bottom electrodes for the respective antifuses 30a, 30b. The top surface of plugs 45 is substantially coplanar with the top surface of the oxide layer 40.

Planar amorphous silicon layer 46 of about 1,600 angstrom thickness is deposited and patterned over the antifuse vias 44. In some embodiments, amorphous silicon layer 46 is deposited by PECVD as described above in connection with Figure 6.

An about 2000 angstrom layer 70 of TiW and an about 8,000 angstrom layer 72 of aluminum-copper are sputter deposited and patterned by standard techniques to form the second metal lines. The portions of layers 70 and 72 over vias 44 form the top electrodes of the respective antifuses 30.

Using standard techniques, a 5,000 angstrom layer of silicon dioxide (not shown) is deposited and pad openings are patterned. Then a 10,000 angstrom layer of silicon nitride (not shown) is deposited and pad openings are patterned. These oxide and nitride layers are used as protective layers. The structure is then alloyed at 400°C using standard techniques.

Aluminum layer 38 provides first level routing channels connected to selected circuit elements of the gate array. TiW layer 70 and AlCu layer 72 provide second level routing channels that are connected to selected circuit elements of the gate array. No additional metal layers are needed to form electrodes of antifuses 30 since the second level channels provide the top electrodes and plugs 45 provide the bottom electrodes. The overall structure of the gate array is thereby simplified, and the number of process steps is reduced.

The second level routing channels extend generally orthogonally to the first level routing channels in a conventional layout shown, for example, in U.S. Patent No. 4,914,055, issued April 3, 1990 to Gordon et al., the disclosure of which patent is hereby incorporated herein by reference thereto. The thick oxide 40 serves to reduce the capacitance between the first level routing channels and the second level routing channels. In spite of the large thickness of oxide layer 40, vias 44 can be made narrow because good quality plugs 45 providing a good contact to aluminum layer 38 can be formed even in narrow vias. Significant size reduction of the gate array is thereby made possible. Leakage current and the capacitance of the unprogrammed antifuse are also reduced thereby.

While the invention has been described with respect to the embodiments included above, other embodiments and variations not described herein may be considered to be within the scope of the invention. For example, the invention should not be limited by the composition of the metal system used for the interconnects, or to any specific thickness of the various films and oxides used in the structure. These other embodiments and variations are to be considered within the scope of the invention, as defined by the following claims.

CLAIMS

What is claimed is:

1. An antifuse structure comprising:

a dielectric layer having an opening therethrough;

a conductive plug filling said opening, a top surface of said plug being substantially coplanar with a top surface of said dielectric layer;

a substantially planar layer of programmable material which is non-conductive when said antifuse structure is unprogrammed and which provides a conductive path therethrough when said antifuse structure is programmed, said layer of programmable material overlaying and contacting said plug; and

a conductor overlaying and contacting said programmable material layer.

2. An antifuse structure as in Claim 1 further comprising a layer of conductive material underlaying and contacting said dielectric layer and said plug.

3. An antifuse structure as in Claim 2 wherein said conductive layer connects said plug to a semiconductor device.

4. An antifuse structure as in Claim 1 wherein said programmable material layer extends at least over the entire top surface of said plug.

5. An antifuse structure as in Claim 1 wherein said programmable material layer has a substantially planar portion extending at least over the entire top surface of said plug.

6. An antifuse structure as in Claim 1 wherein said conductor has a portion directly above said plug.

7. An antifuse structure as in Claim 6 wherein said portion is substantially planar and wherein said portion extends at least over the entire top surface of said plug.

8. An antifuse structure as in Claim 1 wherein said plug completely fills said opening.

9. An antifuse structure as in Claim 1 wherein said plug comprises tungsten.

10. An antifuse structure as in Claim 28 wherein said amorphous silicon is about 1,600 angstroms thick.

11. An antifuse structure as in Claim 1 wherein said dielectric layer is about 9,000 angstroms thick.

12. An antifuse structure as in Claim 28 wherein said conductor comprises:

a layer of TiW; and

a layer of aluminum separated from said programmable material layer by said layer of TiW.

13. A method for fabricating an antifuse structure, comprising the steps of:

fabricating an insulating layer;

fabricating an opening through said insulating layer at a selected location;

fabricating a plug of conductive material in said opening so that a top surface of said plug is substantially coplanar with a top surface of said insulating layer;

fabricating a layer of amorphous silicon overlaying and contacting said plug; and

fabricating a conductor overlaying and contacting said amorphous silicon layer.

14. A method as in Claim 13 wherein said conductive

material comprises tungsten.

15. A method as in Claim 13 wherein said step of fabricating a plug comprises the steps of:

depositing a first layer of conductive material over said insulating layer and into said opening, said first layer having a substantially planar top surface; and

etching at least a portion of said first layer so as to fabricate said plug.

16. A method as in Claim 13 wherein said step of fabricating a plug comprises the step of selectively depositing conductive material into said opening.

17. A method as in Claim 13 further comprising the step of fabricating a conductive layer underlaying said insulating layer and contacting said plug.

18. A method as in Claim 17 wherein said step of fabricating a conductive layer precedes said step of fabricating an insulating layer.

19. A method as in Claim 13 wherein said step of fabricating a layer of amorphous silicon comprises the step of depositing amorphous silicon using PECVD.

20. A method as in Claim 13 wherein said step of fabricating a conductor comprises the steps of:

depositing a layer of TiW; and

depositing a layer of aluminum so as to separate said amorphous silicon layer from said layer of aluminum by said layer of TiW.

21. A method as in Claim 20 wherein

said step of depositing a layer of TiW comprises the step of depositing TiW using sputtering; and

said step of depositing a layer of aluminum comprises the step of depositing aluminum using sputtering.

22. A programmable integrated circuit comprising:

a semiconductor structure having circuit elements in a substrate;

a first level of conductive routing channels, said first level channels being connected to selected circuit elements;

an insulating layer overlaying said first level routing channels, said insulating layer having openings formed therein at selected locations;

a conductive plug in each of said openings, each plug contacting said first level routing channels, a top surface of said insulating layer having, for each plug, a portion adjacent the respective plug, each portion being substantially coplanar with a top surface of the respective plug;

a layer of programmable material overlaying and contacting said plugs, said programmable material being non-conductive when said integrated circuit is unprogrammed, said programmable material providing one or more conductive paths therethrough when said integrated circuit is programmed, said programmable material layer having, for each plug, a substantially planar portion which overlays the plug and also overlays the respective adjacent portion of the top surface of said insulating layer; and

a second level of conductive routing channels, said second level channels being connected to selected circuit elements, said second level channels overlaying and contacting said programmable material layer at said selected locations.

23. A programmable integrated circuit as in Claim 22, wherein said openings terminate at said first level

routing channels.

24. A programmable integrated circuit as in Claim 22, wherein said insulating layer is about 9000 angstroms thick.

25. A programmable integrated circuit as in Claim 22, wherein said second level channels are substantially orthogonal to said first level channels.

26. A method for fabricating a programmable integrated circuit, comprising the steps of:

forming circuit elements in a substrate;

forming a first level of conductive routing channels, said first level channels being connected to selected circuit elements;

forming an insulating layer overlaying said first level routing channels;

forming openings through said insulating layer at selected locations and terminating said openings upon selected ones of said first level routing channels;

forming a conductive plug in each of said openings, a top surface of each plug being substantially coplanar with a portion, surrounding the plug, of a top surface of said insulating layer, each plug contacting said first level routing channels;

depositing a layer of amorphous silicon so that said amorphous silicon contacts and overlays said plugs; and

forming a second level of conductive routing channels, said second level channels being connected to selected circuit elements, said second level channels contacting and overlaying said amorphous silicon.

27. A method as in Claim 26 wherein said second level channels are substantially orthogonal to said first level channels.

28. An antifuse structure as in Claim 1 wherein said programmable material comprises amorphous silicon.

29. An antifuse structure as in Claim 1 wherein said conductor comprises:

a layer of conductive material; and

a barrier layer separating said conductive material from said programmable material for preventing the conductive material from spiking into said programmable material.

30. A programmable integrated circuit as in Claim 22 wherein said programmable material comprises amorphous silicon.

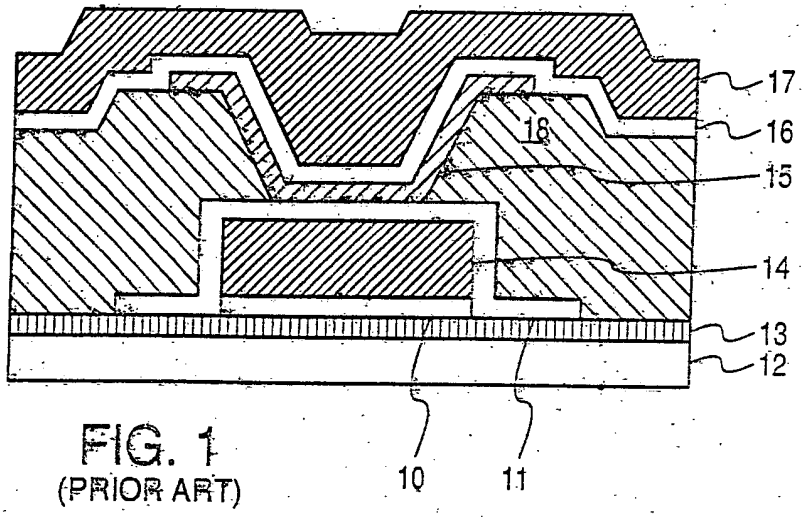

FIG. 1
(PRIOR ART)

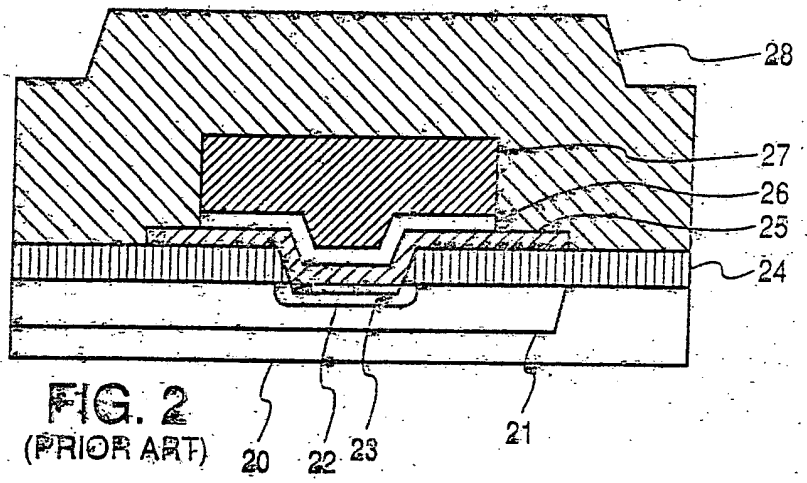

FIG. 2
(PRIOR ART)

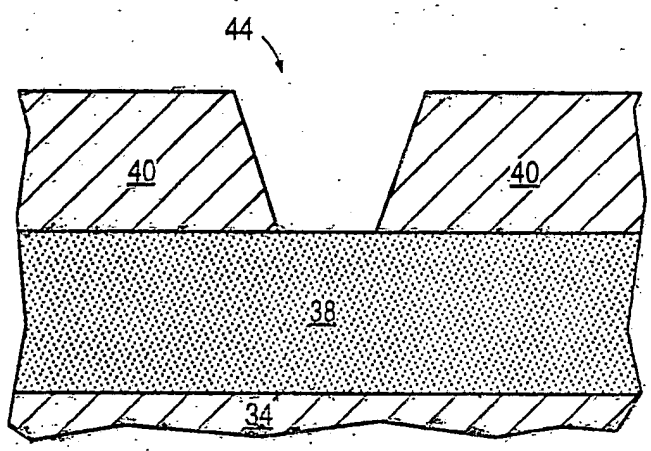

FIG. 3

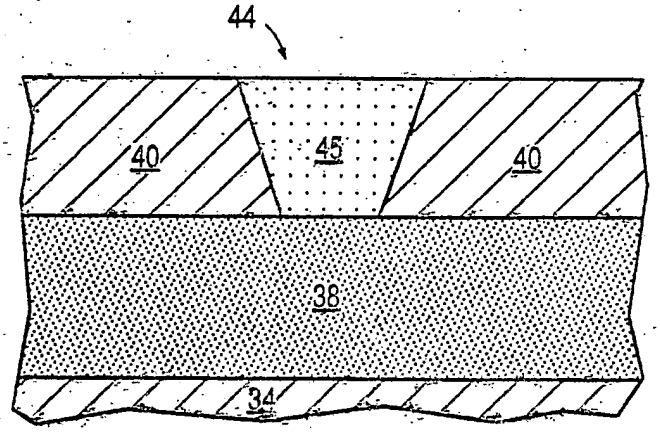

FIG. 4

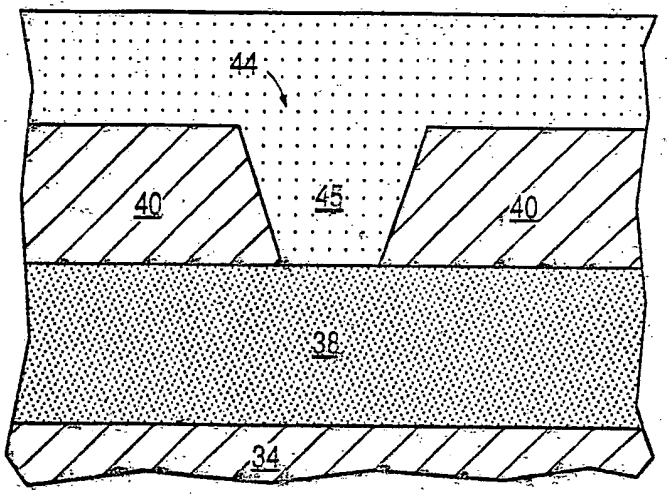

FIG. 5

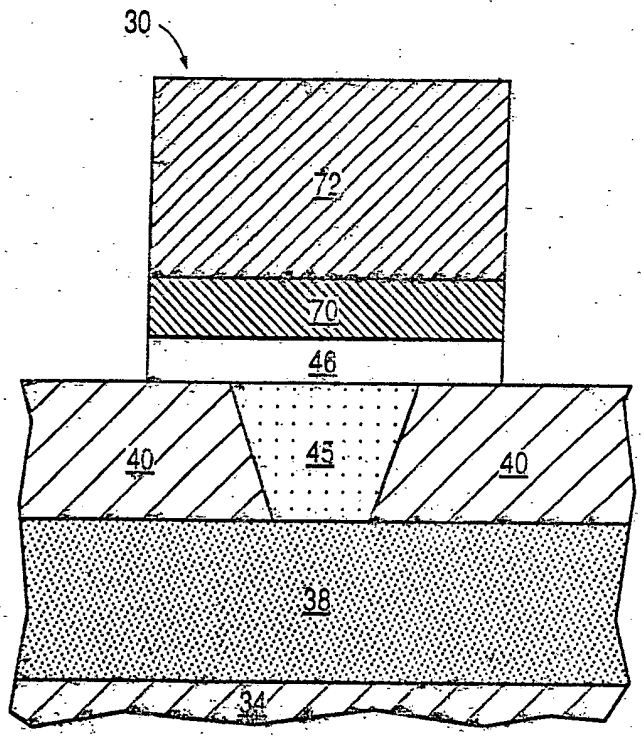

FIG. 6

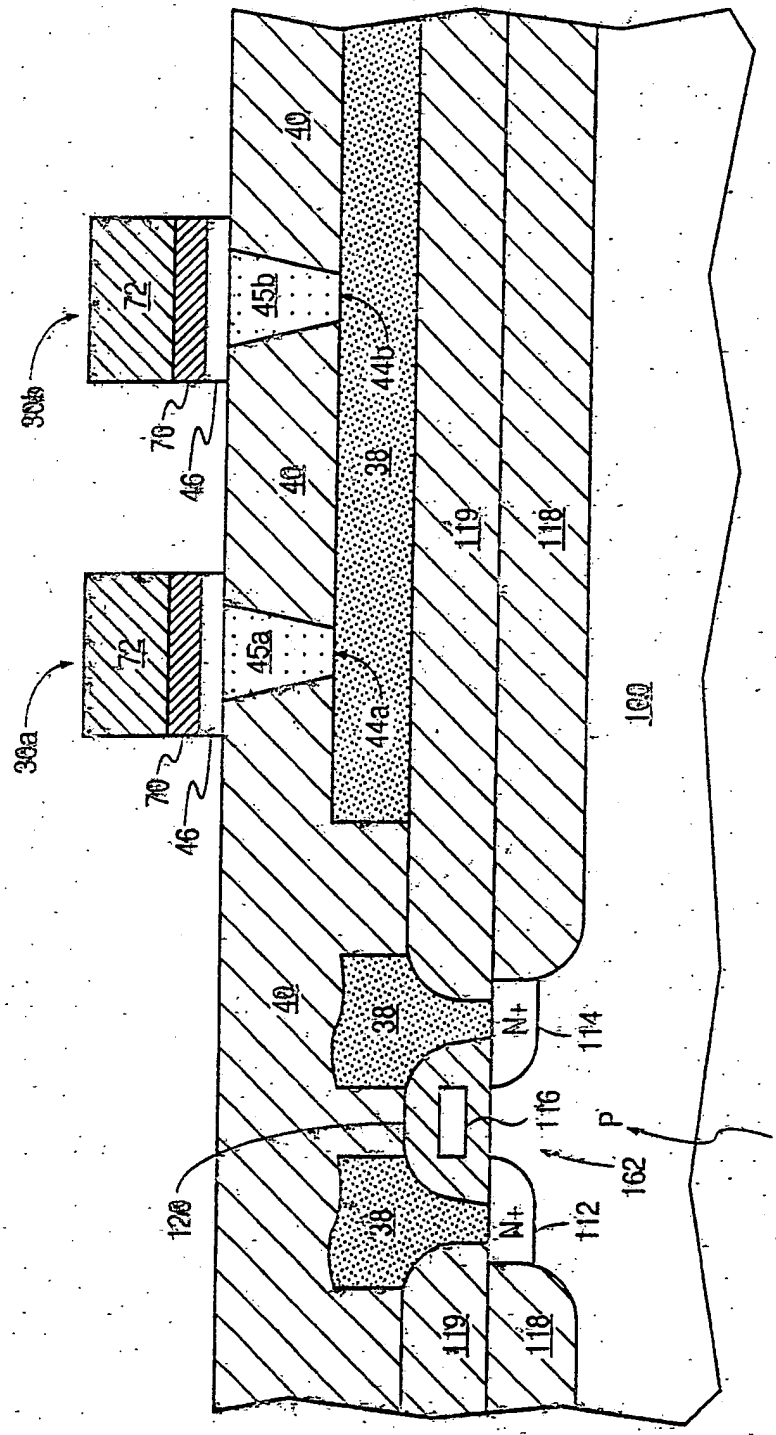
40
72
45b
44b
30b
70
46
38
119
118
72
45a
44a
30a
70
46
100
40
38
N+
114
116
P
104
162
120
38
N+
112
119
118

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/03919

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 45/00,27/02,23/48,21/44,21/465.
US Cl. :357/2,51,67,71;437/192,203,228,245

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 357/2,51,67,71;437/192,203,228,245

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 4,933,898 (Gilberg et al.) 12 June 1990, see figure 2.	1-8,22,23,25, 27
X Y	US,A, 4,922,319 (Fukuakima) 01 May 1990, see figure 7(a) to 7(g)	1-8,11,13-24 26,27 9,10,12,25, 28-30
Y	US,A 4,847,732 (Stopper et al) 11 July 1989, see figure 16.	29
Y	US,A, 4,499,557 (Holmberg et al.) 12 February 1985 see column 9, lines 50-58 and figure 5.	10,12,19-21,26,27
Y	US,A, 4,458,297 (Stopper et al.) 03 July 1984 see figure 8.	1-8,22,23,25
Y	US,A, 4,424,578 (Miyamoto) 03 January 1984 see column 4, lines 3-22.	10,19,26, 28,30
Y	US,A, 3,675,090 (Neale) 04 July 1972, see line 1, column 6.	11,24

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 AUGUST 1992	02 OCT 1992
Name and mailing address of the ISA/ Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer J. CARROLL Telephone No. (703) 308-4926

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